A NEW CMOS CHARGE PUMP FOR LOW VOLTAGE APPLICATIONS

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ABSTRACT

A new charge pump, which can operate with very low supply voltages, is proposed. The MOS transistors are used as charge transfer switches (pass gates) to eliminate the effect of the threshold voltage in the pumping gain of each stage. The MOS switch of each pumping stage is controlled by the output of a dynamic inverter established in the same stage; however, the control voltage of that inverter is derived from the preceding stage. This forward control scheme considerably reduces the risk of reverse current and eliminates the need for extra circuitry, which is necessary for establishing the initial node voltages. Simulation results show that the proposed charge pump has higher pumping gain compared to other published charge pumps.

I. INTRODUCTION

Power consumption is one of the most crucial considerations in designing a VLSI system. Generally, the most common and efficient method to reduce the power consumption in a digital system is to reduce the power supply voltage. However, a low supply voltage can considerably reduce the quality of the circuit function. In fact, it causes a reduction in speed and noise margins in digital circuits, a reduction in dynamic range of analog circuits and some difficulties in read and write operation in some types of memories such as EEPROM or Flash types [1].

Charge pumps are circuits, which can generate a voltage higher than the regular supply voltage or a voltage of reverse polarity. Most MOS charge pumps are based on the Dickson charge pump [2], which is shown in Fig. 1. The MOS transistors in Fig. 1 work as diodes; so the charge can be pushed in only one direction. The output voltage of the Dickson charge pump is:

$$V_{out} = \sum_{i=0}^{N} (V_{DD} - V_{t,Mi}) \qquad (1)$$

where V_{DD}-$V_{t,Mi}$ is the voltage gain of the *ith* stage and N denotes the number of stages. Although the Dickson charge pump has relatively good performance with reasonable supply voltages and some special process technologies [3], it has two major drawbacks when working with

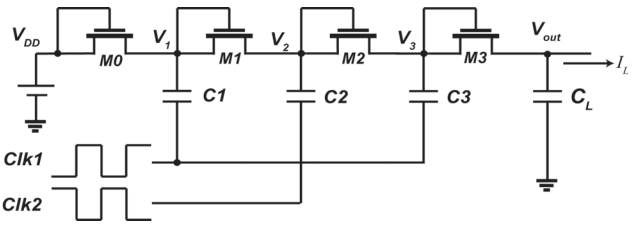

Fig. 1. A three-stage Dickson charge pump.

low supply voltages. Firstly, since the threshold voltage of MOS transistors does not scale with supply voltage, the voltage gain of each stage becomes very small with very low supply voltages. Secondly, since the voltage at each stage is increased from the previous stage by the charge pumping effect, the threshold voltage of the diode connected MOS transistors increases due to the body effect. As a result, the voltage gain decreases as the number of stages increases. These two drawbacks prevent the generation of high voltages from very low power supply voltages, even if the number of stages is increased.

To reduce the pumping voltage loss due to body effect and threshold voltage, several circuit topologies have been published in the literature. The use of floating-well devices to mitigate the body effect is reported in [4], however the resulting charge pump may generate substrate current by having floating devices, and only solves the body effect problem, not voltage loss due to threshold voltage. Controlling the voltage of the body terminal of MOS switches to avoid the body effect problem is proposed in [5], however this method still suffers from the voltage loss due to threshold voltage.

The use of MOS transistors as charge transfer switches has been proposed to mitigate the above problems. The method presented in [6] is based on the backward control of MOS switches. This approach has the risk of reverse current and also requires an additional circuit to generate high-voltage clocks for the final pumping stage. Another problem is that the backward control operation produces some problems during start-up so that extra circuitry is needed for setting up the initial voltage at each pumping node. Two ×4 and ×6 charge pumps based on voltage doubler approach are presented in [7]; however, for their proper operation, some limitations are imposed on the body effect coefficient, which are not met in many CMOS technologies.

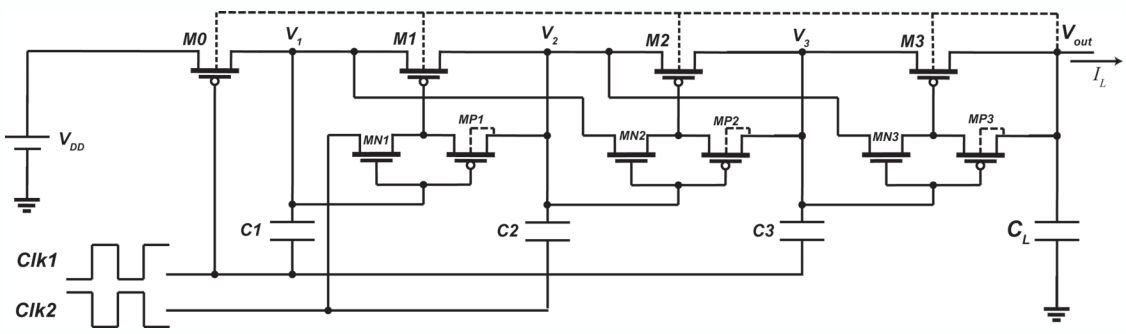

Fig. 2. The basic schematic of the new three-stage charge pump (the bulk of all nMOS transistors is connected to ground).

In this paper, a new charge pump circuit is presented which uses PMOS transistors as switches. It will be shown that this circuit eliminates the effect of the threshold voltage of MOS switches and generates an output voltage which is almost equal to the ideal value $(N+1)V_{DD}$. Section II of this paper presents the idea of the new charge pump circuit and explains about its operation. Section III discusses modifications to the circuit required for perfect operation. Section IV provides some simulation results and compares the new charge pump with some of other well-known charge pumps. It will be shown that much higher pumping gain can be achieved compared to other charge pumps working on the Dickson charge pump principle. Finally, Section V presents the conclusions.

II. OPEARATION PRINCIPLE OF THE PROPOSED CHARGE PUMP

A MOS switch when is completely on can pass charge from its drain to its source similar to a forward biased diode; however, it has the advantage that almost no voltage drop occurs between its drain and source terminal. We take advantage of this by replacing the diode connected nMOS transistors of a classical Dickson charge pump with pMOS switches (Fig. 2). If these switches are turned on and off at proper clock phases, they can allow the charge to be pushed in only one direction.

In order to control the on/off operation of each switch, a dynamic inverter is inserted in each stage. The inverter works dynamically because its low and high voltages change during different clock phases and are different from the low and high voltages of the inverters of the other stages. The control voltage of each inverter is derived from the pumping node of the preceding stage; i.e. a forward control scheme is used where the voltage at each pumping node controls the on/off operation of the next stage.

The basic operation of the charge pump, in steady-state mode with no load and ideal conditions (no parasitic), can be seen in Fig. 3 where we show the voltage waveform of each pumping node and nonoverlapping clocks, *Clk1* and *Clk2*. With references to Figs. 2 and 3, the operation of the second stage of the charge pump, as an example of other stages, is as follows:

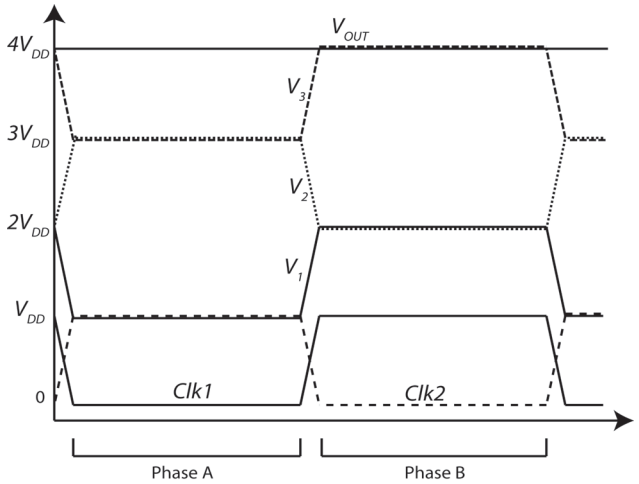

Fig. 3. Clocks and node voltages waveforms in steady state mode with no load and ideal conditions (no parasitic).

Based on the Dickson charge pump operation, during phase A, *Clk1* is low and *Clk2* is high, *M0* and *M2* are turned on and able to pass charge to their following stages and *M1* and *M3* should be turned off to impede reverse current. Therefore, during this phase $V_1=V_{DD}$, $V_2=V_3=3V_{DD}$ and $V_{out}=4V_{DD}$. As a result, the V_{GS} of transistor *MP2* is equal to zero and the output of the inverter *MN2-MP2* is low; i.e., V_{DD}. Hence, the V_{GS} of PMOS transistor *M2* is equal to $-2V_{DD}$, which confirms the supposition that *M2* is on.

During phase B in which *Clk1* is high and *Clk2* is low, *M1* and *M3* should be turned on to be able to pass the charge to their following stages and *M0* and *M2* should be off to impede the reverse current. Hence during this phase $V_1=V_2=2V_{DD}$, $V_3=V_{out}=4V_{DD}$. As a result, the V_{GS} of transistor *MN2* is equal to zero and the output of the inverter *MN2-MP2* is high; i.e., $4V_{DD}$, which means the V_{GS} of pMOS transistor *M2* is equal to zero, verifying that transistor *M2* is off, as we supposed.

During start-up, since the node voltages of all pMOS switches are zero, they can pass charge to their following stages. In addition, we can see from the cross-section view of Fig. 4 that at start-up, the output voltage is less than

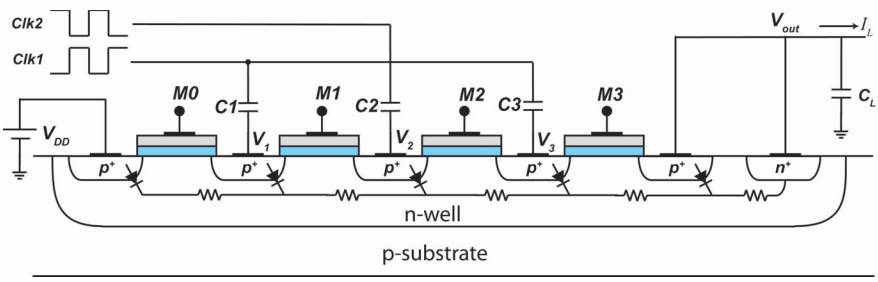

Fig. 4. Cross-section view of the three-stage charge pump depicted in Fig. 2

the power supply voltage and internal pumping node voltages, so that the diodes between the p+ diffusion of pMOS switches and n-well are forward biased and also pass charge to the output node. However, at steady-state operation, the output voltage is high enough to cause these diodes to become reverse biased.

III. CIRCUIT DESIGN ISSUES

The charge pump circuit discussed in the previous section has two problems. The first one happens during start-up. Referring to Fig. 4, during start-up the output voltage is less than power supply voltage and internal pumping node voltages. Hence, the diodes formed between the p+ diffusion of the pMOS switches and the n-well are forward biased and pass current to the well (the output node). If the parasitic resistance of the n-well is low, the forward current through those diodes may become damagingly large. This problem can be easily avoided, by proper circuit layout. That is, by increasing the distance between the p+ diffusions and n+ contact of the n-well, the parasitic resistance of n-well increases and limits the bulk current. For more protection, a small resistor R_B, can be inserted between bulk terminal and output (Fig. 5).

In addition, the current flowing to n-well through p+ diffusions during start-up may cause latch-up in the circuit. As a result, proper layout techniques should be used to improve latch-up immunity of the circuit.

The second problem is associated with the first pMOS switch *M0* in steady-state mode. As explained in the previous section, during phase B, when *Clk1* is high and *Clk2* is low, the transistor *M0* should be off to impede the reverse current from node V_1 to V_{DD}. However, since in steady-state mode the voltage across capacitor *C1* is close to V_{DD}, therefore when *Clk1* goes high, the voltage difference between node V_1 and the gate terminal of transistor *M0* is approximately V_{DD}. As a result, this transistor is still on and can pass reverse current. This problem is due to the forward control scheme used in this circuit; i.e., no voltage control exists to properly control the on/off operation of the first switch.

To solve this problem the pMOS switch *M0* is replaced by an nMOS switch and a dynamic inverter. The control voltage for the inverter comes from node V_1, which means that a backward control scheme is used for the first switch. As a result an additional diode-connected transistor, *MD,* is inserted to establish the initial voltage at node V_1. The operation of NMOS switch *M0* and its controlling inverter *MN0-MP0* is similar to the operation of other stages, as explained in Section II.

It is worth noting that if all of the switches are realized by nMOS transistors, two problems will arise. Firstly, since the control voltage for the dynamic inverters has to come from the following stages (backward control), there is no node voltage to control the operation of the last pumping stage. As a result, a high voltage clock generation circuit is necessary to control the on/off operation of the last stage. Secondly, some additional diode-connected transistors are necessary to establish node voltages during start-up. Therefore, by using nMOS switches circuit will be more complex and less efficient.

The schematic of the modified circuit is shown in Fig. 5. A concluding remark is that since all the MOS switches are turned on with V_{GS} approximately equal to $2V_{DD}$, as long as the threshold voltage of the switches is less than $2V_{DD}$, this circuit operates perfectly. This is another important advantage for this circuit compared with other topologies, which requires that the transistor threshold voltages be less than V_{DD}.

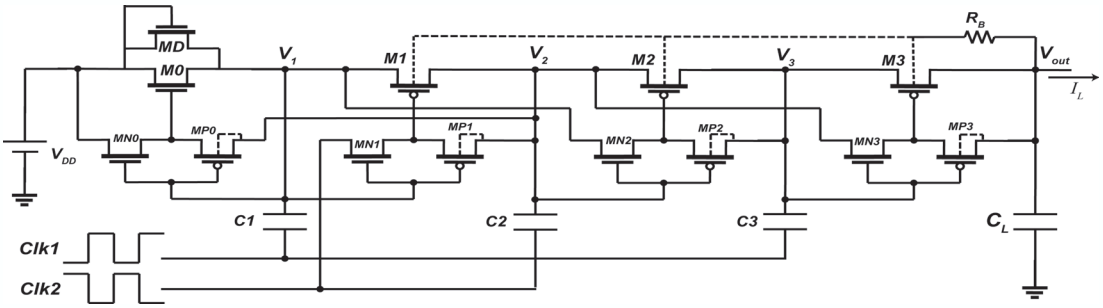

Fig. 5. The schematic of the modified three-stage charge pump (the bulk of all nMOS transistors is connected to ground).

IV. SIMULATION RESULTS

The proposed charge pump was designed in a 0.35μm CMOS process. The junction breakdown voltage (B.V.) limit is 8.0 V in this process. The threshold voltage V_{t0} is 0.55 V and -0.7 V for nMOS and pMOS transistors, respectively. The value of coupling and output capacitors were chosen to be 15pF and 30pF, respectively. For all simulations the clock frequency was set to 10 MHz.

To show the effectiveness of the new charge pump, other well known charge pumps, based on the Dickson charge pump, were also designed and simulated with the same values for coupling and output capacitors; all of the charge pumps layout area was approximately the same size. Fig. 6 shows the output voltage of the different charge pumps versus the number of stages, N, with no load condition, $I_L=0$, and V_{DD}=1.0 V. From the graph we can clearly see that the proposed charge pump has a much higher pumping gain compared with the others. Indeed, the output voltage of the proposed charge pump is almost equal to the ideal value, $(N+1)V_{DD}$.

Fig. 7 shows the output voltage versus input supply voltage for a three-stage charge pump of the different topologies. This figure shows that output voltage of the new charge pump linearly increases with the input supply voltage with a coefficient of 4. Finally, Fig. 8 shows the output voltage of the proposed charge pump versus load current for different input supply voltages.

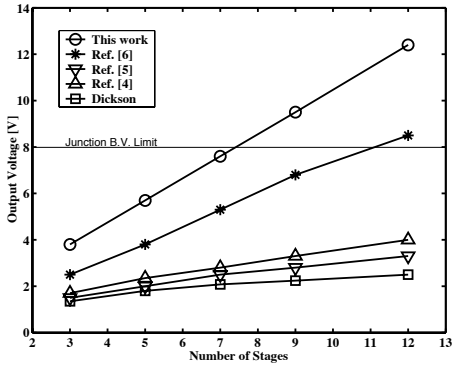

Fig. 6. Output voltage of various charge pumps versus number of pumping stages when I_L=0, and V_{DD}=1.0 V.

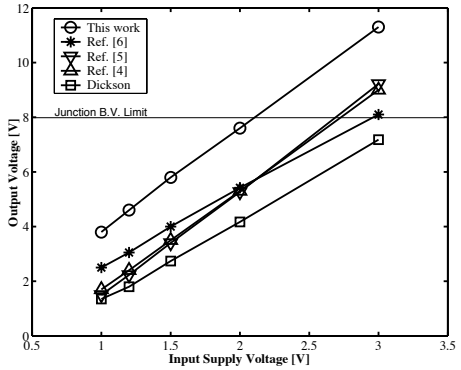

Fig. 7. Output voltage versus input supply voltage of various three-stage charge pumps with when I_L=0.

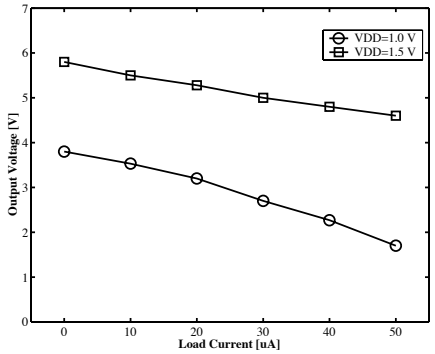

Fig. 8. Output voltage of the new charge pump versus load current for the different input supply voltages.

V. CONCLUSIONS

A new charge pump, which uses MOS transistors as charge transfer switches, has been designed. This approach eliminates the effect of the threshold voltage in the pumping gain of each stage. The MOS switch of each pumping stage is controlled by the output of a dynamic inverter established in the same stage. The forward control scheme used in this new charge pump considerably reduces the risk of reverse current and eliminates the need for extra circuitry which is required for establishing the initial node voltages. It has been shown that a much higher pumping gain can be achieved by this new charge pump compared with other charge pumps working on the Dickson charge pump principle.

VI. REFERENCES

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